07-03-01

2815

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventors	Huili Shao Susan Vitkavage Allen Yen	Case: Shao 10-3
Serial No.	09/464811	Group Art Unit: 2815
Filing Date	December 17, 1999	Examiner: L. Cruz

Title: Integration of Low Dielectric Material in Semiconductor Circuit Structures

#8
7-12-01
Paylor

ASSISTANT COMMISSIONER OF PATENTS
WASHINGTON, D.C. 20231

SIR:

APPELLANT'S BRIEF UNDER 37 C.F.R. 1.192

Appellants hereby appeal the Examiner's rejections in the Final Office Action mailed 01/03/01. Three copies of this brief are transmitted herewith. A Petition for an Extension of Time was filed on June 27, 2001 and a copy is attached hereto.

1. IDENTIFICATION OF THE REAL PARTY IN INTEREST

The real party in interest for the above-identified application is Agere Systems, Inc. which is the assignee of the assignee of record for this application, Lucent Technologies, Inc.

2. IDENTIFICATION OF RELATED APPEALS OR INTERFERENCES

To the best of appellant's knowledge, there are no appeals or interferences that will be directly affected by or will have a bearing on the decision on appeal.

3. STATUS OF THE CLAIMS

Claims 1 – 33 are pending in the application. Claims 22 – 33 have been withdrawn, but not cancelled, under a restriction requirement traversed by applicants. A petition to over rule the restriction requirement made final by the examiner is now pending.

Claims 1 – 21 have been examined and are the subject of this appeal. Claims 1, 5 and 7 were amended during prosecution only for the purposes of adding clarity and to assure compliance with Section 112. None of the amendments narrow the scope of the claims, literally or under the doctrine of equivalents.

A copy of the claims as amended is attached hereto as Appendix A. Appellants respectfully appeal the rejections of claims 1 – 21.

4. STATUS OF THE AMENDMENTS

No amendments were made to the claims after final rejection.

5. BACKGROUND

It is well known that improved electrical performance of high speed integrated circuit devices can result from reductions in capacitive coupling between adjacent levels of metallization. That is, the thickness and dielectric constant of insulator between levels of interconnect wire influence the extent of this coupling. Numerous low dielectric constant ("low k") insulative materials are becoming available as substitutes to conventional high dielectric constant ("high k") materials such as silicon dioxide or silicon nitride. High k materials have dielectric constants ranging above 4.0 while some of the newer low k materials have dielectric constants ranging from about 3 to 1.5.

Unfortunately, the physical properties of such low k materials do not permit their direct substitution for a high k material. By way of example, several of the low k insulators are so soft or flaky they cannot be polished with conventional techniques. Instead, to effect planarization of a low k dielectric layer prior to formation of the next overlying metallization level, a more rugged capping material is deposited over the softer material. The more rugged material is a high k dielectric positioned as the planarizing sublayer over a low k sublayer. The rugged material is typically a conventional dielectric such as the high k dielectric silicon nitride.

With this planarizing requirement it has not been possible to manufacture an integrated circuit structure with a single low k insulative material extending from a first level of

interconnect to a next level of interconnect. Rather, it has been necessary to position at least one intervening high k dielectric layer between the first and second levels as well. That is, the first low k dielectric material at best extends from the lower first level of interconnect up to a rugged, high k capping layer. The capping layer separates the first low k dielectric material from the second level of interconnect and has some effect on interlevel capacitive coupling.

A simplified view of a prior art low k interconnect structure incorporating such a high k capping material is shown in Figure A, attached hereto. This partially fabricated structure is shown to have three levels of Al interconnect runners M1, M2 and M3 formed over a semiconductor substrate layer suitable for formation of transistors. Pairs of runners on adjacent levels may be connected with a conductive via or plug, sometimes formed of Tungsten.

Still referring to Figure A, a conventional dielectric layer D1, e.g., a silicon oxide, is formed between the silicon substrate and the first level of interconnect members. Interconnect runners M1 are formed thereon. A low k dielectric material e.g., hydrogen silsesquioxane (HSQ), k=3.0 approx., is formed between and over the runners M1. A rugged high k capping layer, e.g., Si_3N_5, has been formed over the low k material and planarized to accommodate the second level of runners M2. One or more vias are formed through the high k and low k materials to create a contact to one or more runners M1. Second and third levels of interconnect runners are formed in a manner similar to that described for the runners M1. The resulting prior art structure comprises alternating layers of high k and low k dielectric to insulate the various levels of runners. Note, the low k dielectric is positioned between and over runners on one level to reduce capacitance between conductors on that same level, e.g., M1, as well as between runners on different levels, e.g., M1 and M2. However, the low k dielectric does not extend from *between* runners on one level, e.g., M1, to *between* members on the next level, e.g., M2, because of the intervening high k capping layer.

5. SUMMARY OF THE INVENTION

Generally, the invention is directed to a structure which allows low k insulator material to extend from one level of interconnect runners to an overlying level of interconnect runners as well as between interconnect runners on the same level. Such a structure may be formed by first fabricating two or more metallization levels with conventional high k dielectric material, e.g., silicon oxide; etching some or all of the high k dielectric material from the structure to form voids and then depositing low k dielectric material in voids between some of the interconnect members.

According to claim 1, a first upper level of interconnect members is formed over the semiconductor layer and at least one lower level of interconnect members is formed between the semiconductor layer and the first upper level of interconnect levels. A first insulative material, having a relatively low dielectric constant, electrically isolates members of the first upper level from one another and extends to the lower level of interconnect members. A second insulative material, having a relatively high dielectric constant is positioned to electrically isolate members of the lower level from the electronic device.

According to claim 20 a first upper level of interconnect members is formed over a semiconductor layer and a lower level of interconnect members is formed between the semiconductor layer and the first upper level of interconnect members. An insulative material is positioned to electrically isolate portions of the upper level of interconnect members from one another, and isolate portions of the upper level of interconnect members from portions of the lower level of interconnect members and isolate portions of the lower level of interconnect members from one another. The insulative material comprises a continuous layer extending from within regions between members of the upper level of interconnect to within regions between members of the lower level of interconnect. The continuous layer is characterized by a dielectric constant less than 3.9.

6. ISSUES

The issues on appeal are whether the claims are patentable over U.S. Patent No. 5, 818, 111 (Jeng '111). The appealed claims do not stand or fall together. Rather, each claim defines subject matter which further distinguishes the invention over the art of record.

7. GROUPING OF CLAIMS

For purposes of this appeal all of the claims are grouped together with regard to the one ground of rejection under 35 U.S. Section 102.

8. ARGUMENT

Claims 1-21 have been rejected under Section 102 based on Figure 3 of Jeng '111. It is submitted that all of the claims are distinct and non-obvious over Jeng, alone or in combination with the other art of record.

Jeng '111 concerns prevention of cracks in low dielectric constant materials used in combination with traditional intermetal dielectric materials. See Col. 1, lines 7-13. With reference to porous, low k films, the reference teaches that "thick films of such materials can easily crack .. [Col. 2, lines 21-22]" and proposes to solve "the cracking problem by placing a stabilizing layer in between layers of problematic low-k materials, thereby combining the advantages of traditional dielectric and low dielectric constant materials [Col. 2, lines 27 – 30]." See also Col. 2, lines 33 – 40 which teach stabilizing layers of traditional dielectric including SiO_2 and Si_3N_4.

With respect to Figure 2b, Jeng '111 identifies low-k material with reference numeral 18 and a stabilizing layer with reference numeral 20. Jeng also discloses a "thick... SiO_2 interlayer dielectric 22 for planarization [Col. 4, lines 31-33]." By all appearances, this corresponds to the high k capping dielectric illustrated in the simplified prior art Figure A attached to this brief.

It is noted with respect to Figures 2b and 3 of Jeng '111 that "like numerals are used for like and corresponding parts of the various drawings [Col. 3, lines 31-32]." Thus, with respect to Figure 3 (See Col. 4, lines 43-49) Jeng '111 discloses at each level of metallization a sequence of

low-k dieletric material 18 followed by a thick SiO_2 interlayer dielectric 22 for planarization. See also, Figures 1 and 4 of Jeng '111.

It must be noted that 'Jeng '111 does not teach or suggest a low k dielectric which extends from one level of runners up to another level of runners. Nowhere does Jeng '111 disclose, teach or suggest configuring a low k dielectric layer, e.g., such as Jeng's material 18, positioned to isolate runners, e.g., 14, in one level of metallization from each other and extend to runners in another level of metallization. Clearly, this is precluded by the incorporation in Jeng '111 of the prior art interlayer dielectric 22 for planarization, as well as the stabilizing layer 20.

The Jeng '111 reference cannot be applied, alone or in combination with any other art of record to meet the requirements of applicants' claims. By way of illustration, the teachings of Jeng '111 are inconsistent with the requirement of claim 1 for:

"a first insulative material, having a relatively low dielectric constant, positioned to electrically isolate members of the first upper level from one another and extending to the lower level of interconnect members".

That is, Jeng '111 teaches away from applicants' invention by requiring the stabilizing layer 20 as well as the prior art interlayer dielectric 22."

A similar inconsistency exists between Jeng '111 and the requirement of claim 20 for

"insulative material positioned to electrically isolate portions of the upper level of interconnect members from one another, portions of the upper level of interconnect members from portions of the lower level of interconnect members and portions of the lower level of interconnect members from one another,

said insulative material comprising a continuous layer extending from within regions between members of the upper level of interconnect to within regions between members of the lower level of interconnect, said continuous layer characterized by a dielectric constant less than 3.9."

Any attempt to use the disclosure of Jeng '111 to meet the terms of claim 20 would require a piecemeal reconstruction which is inconsistent with the very teachings of this reference: in combination with a low k material - both a stabilizing layer 20 and an interlayer dielectric 22 for planarization.

The examiner's rejection of claim 1 incorrectly states that a low k material 18 of Jeng '111 is "positioned to electrically isolate members of the first upper level... extending to the lower level of interconnect members ..." Such is precluded by the dielectric 22. Further, the examiner erroneously states the location of dielectric 22 as "positioned to electrically isolate members of the lower level from the electronic device ..."

Similar misreadings of Jeng '111 have been applied to reject claim 20. The rejection merely paraphrases the claim language to conclude that material 18 isolates "portions of the upper level of interconnect members (14) from ... portions of the lower level of interconnect members ..." Such is precluded by high-k dielectric 22. Other errors abound.

In response to applicants' argument that the rejections are in error the examiner has only provided conclusory remarks such as "Layer 18 satisfies the structural requirements of Applicant's claims and '111's SiO layer reads on the claims as drafted..."

Since the examiner has never addressed the inconsistency between Jeng '111 and the claims (as pointed out at pp 6-7 in the Amendment of October 20, 2000) the undersigned requested a telephone interview. Although the examiner was courteous, she refused to discuss the substantive issues and only suggested that the applicants file a continuing prosecution application. Applicants are at a complete loss with regard to how the examiner can conclude that the claims are anticipated. Since Jeng '111 on its face can neither anticipate nor render the claims obvious, and since the examiner refuses to explain how she can possibly apply to the reference to reject the claims, applicants have no recourse except to appeal the decision of the examiner.

It is further submitted that each of the dependent claims further distinguishes the invention over the art of record. For example, in the structure of claim 2 a portion of the second insulative material extends between an interconnect member of the lower level and an interconnect member of the upper level. According to claim 3 the second insulative material predominantly comprises silicon dioxide and the structure further includes a plurality of individual portions formed of the second insulative material, each portion extending between a

member of the lower level and a member of the upper level and self-aligned with said member of the upper level. No art of record discloses these features.

According to claim 4 the structure includes at least a second upper level of interconnect members formed over the first upper level, and the structure of claim 5 further includes a plurality of dielectric supports, formed of the same composition as the lower insulative material, each extending between one of the lower level interconnect members and one of the upper level interconnect members and providing physical support to sustain a spatial relationship between the lower level interconnect members and the upper level interconnect members.

In the structure of claim 6 members of the first level comprise Al, the first insulative material comprises hydrogen silsesquioxane and the second insulative material comprises silicon dioxide. the structure of claim 7 includes a second upper level of interconnect members formed between the first upper level of interconnect members and the lower level of interconnect members wherein portions of the lower insulative material electrically isolate the second upper level of interconnect members from the lower level of interconnect members. The structure of claim 8 further includes a plurality of additional upper levels of interconnect members formed between the first upper level and the lower level, with a first layer formed of the first insulative material and positioned between the first upper level and a first of the additional levels; and a second layer formed of the first insulative material and positioned between second and third ones of the additional levels.

The structure of claim 9 comprises second, third, fourth and fifth upper levels of interconnect members formed between the first upper level and the lower level. In the structure of claim 10 the first, second, third, fourth and fifth upper levels are electrically isolated from one another by a continuous layer comprising the first insulative material. In the structure of claim 11 the first insulative material is a single species of low k dielectric material and the second insulative material predominantly comprises silicon dioxide.

In the structure of claim 12 multiple layers each comprising the first insulative material electrically isolate the first, second, third, fourth and fifth upper levels from one another. In the structure of claim 13 a second upper level of interconnect members is formed between the first level of interconnect members and the lower level of interconnect members wherein portions of the second insulative material extend to electrically isolate the second upper level of interconnect members from the lower level of interconnect members. According to claim 14 portions of the second insulative material extend between two or more of the upper levels.

The structure of Claim 15 further includes a first plurality of conductive portions extending at least between the upper level of interconnect and the lower level of interconnect; and a second plurality of conductive portions extending at least between the lower level of interconnect and some of the electronic devices. In the structure of claim 16 the first plurality of conductive portions are integrally formed with members of the first upper level in a dual Damascene structure.

In the structure of claim 17 all of the members predominantly comprise Al. In the structure of claim 18 the first insulative material extends from the first upper level to electrically isolate members of the lower level from one another. The structure of claim 19 further includes at least a second upper level of interconnect members formed over the first upper level of interconnect members with the first insulative material extending from the first upper level to electrically isolate members of the second upper level from one another.

In the structure of claim 20 the insulative material further includes portions extending between individual members of the upper level and individual members of the lower level, said portions formed of material having a dielectric constant greater than that of said continuous layer. According to claim 21 the insulative material includes portions extending between individual members of the upper level and individual members of the lower level.

9. SUMMARY

Based on the foregoing reasons it is apparent that the examiner's rejections are entirely in error and reversal is therefore requested.

Respectfully submitted,

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Dated: 29 June 2001

APPENDIX A TO APPEAL BRIEF

For Ser. No. 09/464811 (Shao 1-10-3)

CLAIMS ON APPEAL

1(Amended). A semiconductor structure comprising:

a first upper level of interconnect members formed over a semiconductor layer having an electronic device formed thereon;

at least one lower level of interconnect members formed between the semiconductor layer and the first upper level;

a first insulative material, having a relatively low dielectric constant, positioned to electrically isolate members of the first upper level from one another and extending to the lower level of interconnect members; and

a second insulative material, having a relatively high dielectric constant, positioned to electrically isolate members of the lower level from [some of] the electronic device [devices].

2. The structure of claim 1 wherein a portion of the second insulative material extends between an interconnect member of the lower level and an interconnect member of the upper level.

3. The structure of claim 1 wherein the second insulative material predominantly comprises silicon dioxide and the structure further includes a plurality of individual portions formed of the second insulative material, each portion extending between a member of the lower level and a member of the upper level and self-aligned with said member of the upper level.

4. The structure of claim 1 including at least a second upper level of interconnect members formed over the first upper level.

5 (Amended). The structure of claim 1 further including a plurality of dielectric supports, formed of the same composition as the [lower] second insulative material, each extending between one of the lower level interconnect members and one of the upper level interconnect members and providing physical support to sustain a spacial relationship between the lower level interconnect members and the upper level interconnect members.

6. The structure of claim 1 wherein members of the first level comprise Al, the first insulative material comprises hydrogen silsesquioxane and the second insulative material comprises silicon dioxide.

7 (Amended). The structure of claim 1 further including a second upper level of interconnect members formed between the first upper level of interconnect members and the

PRIOR ART – SIMPLIFIED ILLUSTRATION OF LOW K DIELECTRIC INTERCONNECT STRUCTURE USING CONVENTIONAL HIGH K CAP DIELECTRIC INSULATOR (E.G., SiO_2) FOR PLANARIZING LAYER (NOT TO SCALE)

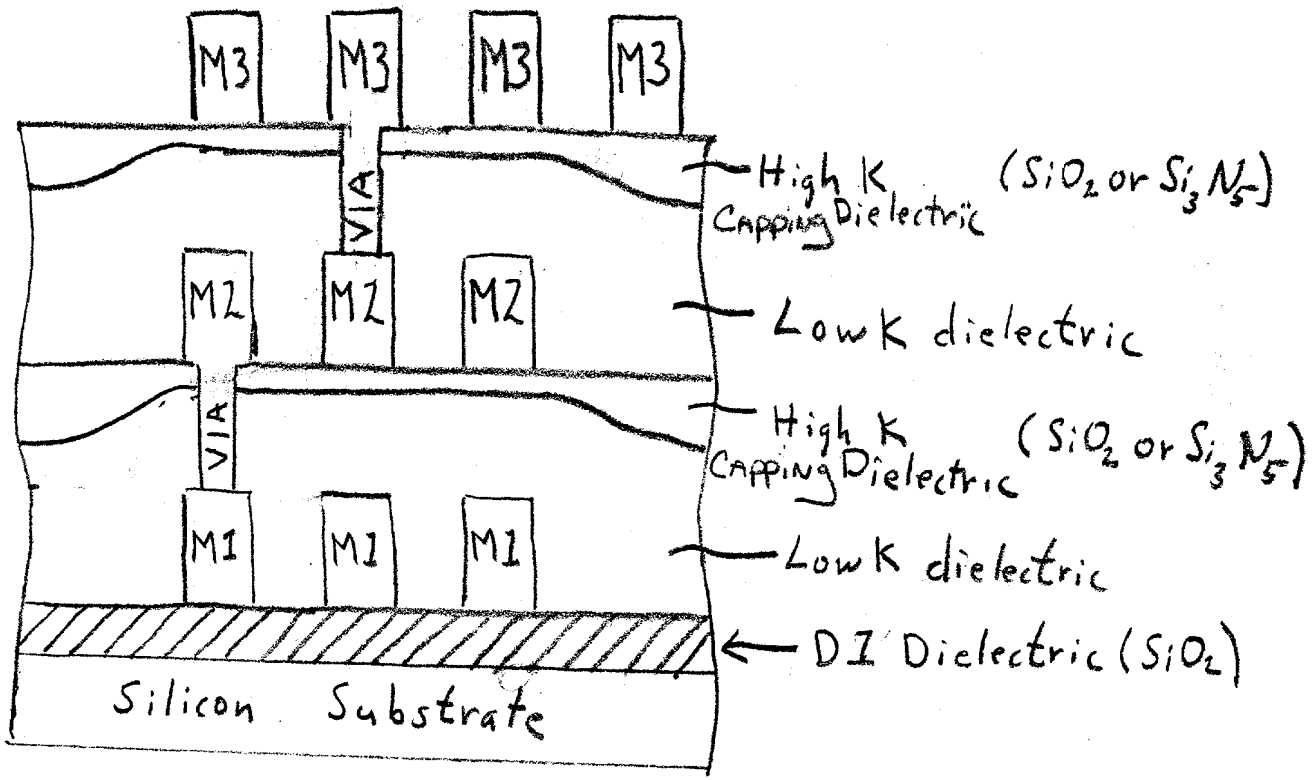

FIGURE A
TO
APPEAL BRIEF
FOR SER. NO. 09/464811

SHAO 1-10-3